UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/687,629 | 10/20/2003 | Satoshi Inoue | 244186US2 | 1805 |

22850 7590 06/11/2007

OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C.
1940 DUKE STREET
ALEXANDRIA, VA 22314

| EXAMINER | |
|---|---|
| PAN, DANIEL H | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2183 | |

| NOTIFICATION DATE | DELIVERY MODE |
|---|---|
| 06/11/2007 | ELECTRONIC |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

patentdocket@oblon.com
oblonpat@oblon.com
jgardner@oblon.com

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/687,629 | INOUE, SATOSHI | |
| | Examiner | Art Unit | |
| | Daniel Pan | 2183 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *29 March 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *7-11 and 17-20* is/are pending in the application.

4a) Of the above claim(s) *1-6 and 12-16* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *7-11 and 17-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *10/20/03,04/28/05,11/01/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

1. Claims 7-11, 17-20 are presented for examination. Clams 1-6, 12-16 have been canceled.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 7-11,17-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mergard et al. (6,401,156) in view of McDonough et al. (5,784,532).

3. As to claims 7, 17, Mergard taught a semiconductor chip (see fig.1, see also the monolithic integrated circuit in col.7, lines 47-59);

a) a processor core (see microcontroller M with the CPU Core) integrated on the semiconductor chip including a general purpose register, an instruction decoder, and a second execution unit [CPU] (see functional parts in the microcontroller M as the functional parts of the processor core fig.1);
b) an extension unit (see Programmable Interrupt controller 48 integrated with M in fig.1) integrated on the semiconductor chip including a first execution unit (see Intel microprocessors 8086 ,80286 in col.7, lines 63-67, col.8, lines 1-9) connected to the processor core;
c) a direct memory access controller (see DMA controller 22 in col.6, lines 20-33) integrated on the semiconductor chip and connected to both the processor core and the

extension unit (see fig.1, see router 168 part of PIC 48 connected to the DMA 22 in col.10, lines 13-36) ;
d) the first execution unit is a reconfigurable first execution unit (see how microcontroller M granted PC/AT functionality of programmable interrupt controller and programmed the PIC functionalities in col.10, lines 1-13).

As to the general purpose registers , see Table 5 [general purpose registers].

4. Mergard did not specifically show the instruction decoder as claimed. However, McDonough taught instruction decoder in a processor core (see col.6, lines 29-36). It would have been obvious to one of ordinary skill in the art to use McDonough for including instruction decoder in Mergard as claimed because the use of McDonough could provide Mergard the ability to decode the instructions in a given processor core for execution and therefore reducing the hardware overheads, and it could be done by reconfiguring the instruction decoder of Mergard into McDonough with modified control parameters (e.g. the R/W ports of the instruction decoder), and because Mergard also taught his processor core (Microcontroller M in fig.1) provided a highly integrated CPU with a complete set of PC/AT mapped peripherals (see col.5, lines 1-8), which was an indication of the applicability of instructing decoder for decoding the CPU commands.

5. As to claim 8, Mergard did not explicitly show the control register and local memory as claimed. However, Mergard, in the same patent, taught his extension unit (programmable controller was a microprocessor 80XX (see Intel microprocessors 8086 ,80286 in col.7, lines 63-67, col.8, lines 1-9). Therefore, Examiner holds that the microprocessor must have a control register and local memory because all these elements, such as control registers, internal RAM had been the standard functional parts of a microprocessor in general (see also the memory for the configuration information in fig.2).

6. As to claim 9,18, examiner holds that instruction decoder logic in the extension unit had to be the same as the reconfigurable logic of first execution unit in order to effectuate the reconfiguration.

7. As to claim 10, 19, Mergard's DMA also connected via an interface to the first execution unit and the DMA (See interface bus in DAM 22 and the first execution unit in fig.1) .

8. As to claims 11,20 see the bus and ISA bus and DRAM and ROM in fig.2.

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Dunning et al. (4,145,739) is cited for the teaching of processor core and extension unit (see fig.2 [8080] and [Master 16]).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 571 272 4172. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 571 272 4162. The fax phone number for the organization where this application or proceeding is assigned is 703 306 5404.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

*21 Century Strategic Plan*

DANIEL H PAN
PRIMARY EXAMINER
GROUP